What is claimed is:

1. A method of implementing a digital communications link connecting a digital controller section of an xDSL modem, located on a system motherboard of a computing system, to a separate analog section of the xDSL modem, located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could significantly affect the overall operation of such said xDSL modem, said method comprising the steps of:

(a) providing a plurality of receive signal lines for communicating data from a remote xDSL modem;

(b) providing a plurality of transmit signal lines for communicating data to a remote xDSL modem;

(c) providing a bit clock signal line for carrying a clock signal, which clock signal is used in connection with communicating said data to and from said remote xDSL modem;

(d) providing a word clock signal to mark the boundary for a sample word received or transmitted on said plurality of receive signal lines and plurality of transmit signal lines.

2. The method of claim 1, further including a step (e): providing a reset signal to ~~reset the analog section of the xDSL modem.~~

3. The method of claim 1, wherein at least four (4) signal lines are used for said receive signal lines, and at least (4) separate signal lines are used for said transmit signal lines.

4. The method of claim 1, wherein the word clock has a cycle consisting of at least four (4) bit clock cycles, with the first cycle being a first value and the remaining ~~cycles being a second value.~~

5. The method of claim 1, wherein said receive and/or transmit signal lines can also be used for implementing an embedded operation channel within said receive and/or transmit signal lines, said embedded operation channel consisting of control signals embedded in both transmit and receive directions for use by the xDSL modem.

6. The method of claim 4, wherein at least one (1) bit per word clock cycle is used to carry control signals.

7. The method of claim 5, wherein each control signal can have either a first or second length.

8. The method of claim 5, wherein each control signal begins with a start bit, is followed by a length bit, then by a set of command bits, and then idle bits are sent between control signals.

9. The method of claim 1, further including a step: providing a multi-channel data frame, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame.

10. The method of claim 9, wherein the number of channels in the multi-channel data frame is programmable.

11. The method of claim 9, wherein the word clock consists of at least four (4) bit clock cycles.

12. The method of claim 11, wherein said same word clock signal is used to mark the boundary of each multi-channel data frame by having a predetermined value for two bit clock cycles at the frame beginning and said word clock signal has said predetermined value for only one bit clock cycle for each word beginning in the rest of the frame.

13. The method of claim 1, wherein said same receive and/or transmit signal lines can also be used to support a data interface between said digital controller and a hardware or DSP based xDSL modem.

14. The method of claim 13, wherein the data interface is logically equivalent to a Utopia I and/or II interface and said hardware or DSP based xDSL modem also can perform an ATM transport convergence (TC) function.

15. The method of 14, wherein an embedded operation channel (EOC) is used to control proper operations of the hardware or DSP based xDSL modem.

16. The method of claim 1, wherein said bit clock signal is based an external master clock operated at a frequency required by said xDSL modem.

17. A communications protocol for transmitting data on an xDSL digital communications link between a digital controller and an analog codec located within a personal computer system, said protocol comprising the steps of:

(a) generating an xDSL bit clock and a separate xDSL word clock adapted for data transmission requirements of said analog xDSL codec;

(b) communicating data words between the digital controller and analog codec at a rate corresponding to said xDSL bit clock;

(c) communicating operational and/or control information embedded within said data words during said word clock period;

wherein both operational and/or control information and data can be simultaneously exchanged between the digital controller and the analog codec.

18. The protocol of claim 17, wherein said operational and/or control information includes information relating to real time control settings for circuits located within the analog codec.

19. The protocol of claim 18, wherein said operational and/or control information further includes information relating to power management for an xDSL modem.

20. The protocol of claim 19, wherein said operational and/or control information consists of control data words that are transmitted asynchronously with respect to data words.

21. The protocol of claim 20, wherein said operational and/or control information consists of a control data word, and wherein a start bit is used within said operational control information to indicate the beginning of a valid control data word.

22. The protocol of claim 17, wherein said data words and operational and/or control information are communicated over a single set of data lines.

23. The protocol of claim 22, further wherein multiple data channels are operated between the digital controller and analog codec on said single set of data lines.

24. The protocol of claim 23, wherein said xDSL word clock has a first duration for data communications in said first data channel, and a second duration for data communications in said second data channel.

25. The protocol of claim 17, wherein the digital controller section is located on a system motherboard of a computing system, and the analog codec is located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could significantly affect the overall operation of such xDSL modem.

26. The protocol of claim 17, further including a step of transmitting embedded control information from the digital controller to the analog codec indicating loss of power in the personal computer system.

27. A communications protocol for transmitting data on an xDSL digital communications link between a digital controller and a plurality of analog codecs occupying a plurality of respective data channels within a personal computer system, said protocol comprising the steps of:

(a) generating an xDSL bit clock and a separate xDSL word clock adapted for data transmission requirements of the plurality of analog xDSL codecs;

(b) communicating data words between the digital controller and the plurality of analog codecs during said xDSL word clock;

(c) grouping multiple data words in a data frame to support the plurality of data channels and/or different accumulated data rates between transmit and receive directions for one or more of the plurality of analog codecs.

28. The protocol of claim 27, wherein said word clock signal is used to mark the boundary of each multi-channel data frame by having a predetermined value for two bit clock cycles at the frame beginning, and said word clock signal has said predetermined value for only one bit clock cycle for each word beginning in the rest of the frame.

29. The protocol of claim 27, wherein operational and/or control information for each of said plurality of codecs is embedded in data words communicated through the plurality of data channels.

30. The protocol of claim 29, wherein said operational and/or control information consists of control data words that are transmitted asynchronously with respect to data words.

31. The protocol of claim 27, wherein the digital controller section is located on a system motherboard of the computing system, and the analog codec is located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could materially affect the operation of such analog codec.

32. A method of implementing a digital communications link within a personal computer system, comprising the steps of:

(a) providing a plurality of receive signal lines, said receive signal lines being configurable such that data can be received by a digital controller from an analog codec and/or a hardware or DSP based xDSL modem with an ATM interface;

(b) providing a plurality of transmit signal lines, said transmit signal lines being configurable such that data can be transmitted by a digital controller to an analog codec and/or a hardware or DSP based xDSL modem with an ATM interface;

(c) providing a clock signal line, said clock signal line carrying a clock signal adapted for data transfers associated with an analog codec and/or a hardware or DSP based xDSL modem with an ATM interface;

(d) providing a data transfer protocol such that data transfers over said digital communications link can include conventional xDSL codec samples and/or ATM cell data.

33. The method of claim 32, wherein said ATM interface is logically equivalent to an ATM Utopia I and II interfaces.

34. The method of claim 33, wherein the digital controller section is located on a system motherboard of the personal computer system, and the analog codec is located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could materially affect the operation of such analog CODEC.

35. The method of claim 32, wherein said digital communications link supports a plurality of data channels by time division multiplexing data transfers using a word clock signal related to said clock signal.

36. The method of claim 32, wherein operational and/or control information for said analog codec and/or hardware/DSP based xDSL modem can be embedded in data words communicated through the plurality of receive and transmit signal lines.

37. A digital controller for use with an xDSL capable modem comprising:

[i] means for processing xDSL formatted data and control signals; and

[ii] means for generating control signals associated with maintaining an xDSL compatible data link; and

[iii] a digital interface for coupling the digital controller to an analog codec associated with said xDSL compatible modem and, said digital interface being configured such that:

[i] a plurality of receive lines can be used for receiving xDSL data; and

[ii] a plurality of transmit lines can be used for transmitting xDSL data;

[iii] a bit clock signal line can be used for carrying a bit clock signal adapted for an xDSL compatible data link; and

[iv] a word clock signal can be used for clocking xDSL data words; and

[v] an embedded control channel is provided so that said control signals can be passed between said digital controller and said analog codec sections of said xDSL capable modem using said plurality of receiving lines and/or said plurality of transmitting lines; and

wherein said digital controller is adapted to be physically placed on a computer motherboard.

38. The digital controller of claim 37, wherein said control signals are asynchronously transmitted with respect to said xDSL data words.

39. The digital controller of claim 37, wherein said digital interface can handle a multi-channel data frame, said multi-channel data frame having at least two data channels, and wherein data can be transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame.

40. The digital controller of claim 37, wherein said control signals relate to real time control settings for circuits located within the analog codec.

41. The digital controller of claim 37, wherein said control signals relate to power management for the xDSL capable modem.

42. An analog codec for use with an xDSL capable modem comprising:

[i] line interface circuitry for coupling to a data channel carrying analog data signals corresponding to xDSL formatted data and control signals; and

[ii] circuitry for performing A/D and D/A operations on said analog data signals and xDSL formatted data and control signals respectively; and

[iii] a digital interface for interfacing to a digital controller located on a computer motherboard, said digital interface being configured such that:

[i] xDSL data signals are received using a first plurality of receiving lines; and

[ii] xDSL data signals are transmitted using a second plurality of transmitting lines; and

[iii] a bit clock signal adapted for an xDSL compatible link can be used by the digital interface; and

[iv] a word clock signal can be used for clocking xDSL data words; and

[v] an embedded control channel for passing control information between said digital controller and said analog codec sections of said xDSL capable modem can be implemented using either or both said plurality of receiving and/or transmit lines; and

wherein said codec is adapted to be physically separated from said digital controller, and placed at a position which is substantially free of electronic noise from other electronic components on said motherboard which could materially affect the operation of such CODEC.

43. The codec of claim 42, wherein said control information is transmitted asynchronously with respect to said xDSL data words.

44. The codec of claim 42, wherein said digital interface can handle a multi-channel data frame, said multi-channel data frame having at least two data channels, and wherein data can be transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame.

45. The codec of claim 42, wherein said control information relates to real time control settings for circuits located within the analog codec and/or analog front circuitry associated with the xDSL capable modem.

46. The codec of claim 42, wherein said control information relates to power management for the xDSL capable modem.

47. An xDSL compatible modem comprising:

(A) a digital controller, said digital controller being adapted so that it can be placed physically on a computer motherboard and further including:

[i] means for processing xDSL formatted data and control signals; and

(B) an analog codec, said analog codec being adapted to be physically separated from said digital controller at a distance sufficient to be substantially free of electronic noise generated by said motherboard, said analog codec further including:

[i] line interface circuitry for coupling to a data channel carrying analog data signals corresponding to said xDSL formatted data and control signals; and

[ii] circuitry for performing A/D and D/A operations on said analog data signals and xDSL formatted data and control signals respectively; and

(C) a digital interface for coupling said digital controller and analog codec, said digital interface including:

[i] a plurality of xDSL data receiving lines; and

[ii]a plurality of xDSL data transmitting lines; and

[iii] a bit clock signal and a word clock signal adapted for an xDSL compatible link; and

[iv] means for providing a control channel data in said xDSL compatible link between said digital controller and said analog codec sections of said xDSL modem

48. The modem of claim 47, wherein said analog codec is located on a riser card which is configured to be mounted substantially perpendicular to said motherboard.

49. The modem of claim 47, wherein said digital controller is implemented in part in software by host processor located on said motherboard.

50. The modem of claim 47, wherein the receive and/or transmit signal lines can also be used for carrying an embedded control word for use by the xDSL modem.

51. The modem of claim 50, wherein said embedded control words can have either a first or second length.

52. The modem of claim 51, wherein a separate data bit of a data word is used for said embedded control word, and said separate data bit is carried on each of said plurality of receive signal lines and/or transmit signal lines during the duration of at least one bit clock signal.

53. The modem of claim 47, further wherein said word clock signal marks the boundary for each sample word received or transmitted on said plurality of receive signal lines and/or plurality of transmit signal lines respectively.

54. The modem of claim 47, wherein at least four (4) signal lines are used for said receive signals, and at least (4) separate signal lines are used for said transmit signals.

55. The modem of claim 47, wherein the word clock signal has a cycle consisting of at least four (4) bit clock cycles, with the first cycle being a first value and the remaining cycles being a second value.

56. The modem of claim 55, wherein at least one (1) bit per word clock cycle is used to carry control signals.

57. The modem of claim 56, wherein each control signal begins with a start bit, is followed by a length bit, then by a set of command bits, and idle bits are sent between control signals.

58. The modem of claim 47, further wherein said digital interface uses a multi-channel data frame, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame.

59. The modem of claim 47, wherein said receive and/or transmit signal lines can also be used to support a compatible data interface for an ATM based hardware xDSL modem.

60. The modem of claim 59, wherein said data interface for the ATM based hardware xDSL modem is logically equivalent to Utopia I and II.

61. In a motherboard for use in a personal computing system, and which system is configured to treat a high speed xDSL capable modem as a motherboard device, the improvement comprising:

(A) a digital controller associated with the high speed modem, said digital controller being located physically on the motherboard and including:

[i] circuitry for processing xDSL formatted data and control signals; and

(B) an analog front end circuit associated with the high speed modem, said analog front end circuit being electrically coupled but physically separated from said digital controller, said analog front end circuit including:

[i] line interface circuitry for coupling to a data channel carrying analog data signals corresponding to said xDSL formatted data and control signals; and

[ii] circuitry for performing A/D and D/A operations on said analog data signals and xDSL formatted data and control signals respectively; and

(C) a digital interface for coupling said digital controller and analog front end circuit, said digital interface including:

[i] a plurality of xDSL data receiving lines; and

[ii]a plurality of xDSL data transmitting lines; and

[iii] a clock signal adapted for an xDSL compatible link; and

[iv] an embedded control channel data in said xDSL compatible link;

wherein said digital interface supports an xDSL compatible data link between ~~said digital controller and said analog~~ front end circuit.

62. The motherboard of claim 61, wherein said analog front end circuit is located on a riser card which is configured to be mounted substantially perpendicular to the motherboard.

63. The motherboard of claim 61, wherein said digital controller is controlled in part in software by a host processor located on the motherboard.

64. The motherboard of claim 61, further wherein said digital interface uses a multi-channel data frame, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame.

65. The motherboard of claim 61, wherein said receive and/or transmit signal lines can also be used to support an ATM interface for a hardware based xDSL modem.

66. The motherboard of claim 61, wherein said ATM interface is a Utopia I and/or II interface.